In the Drawings

The drawings stand objected to because a label appearing in FIG. 3(b) does not correspond to the written description. In this regard, Applicant submits herewith a corrected sheet of drawings, which includes a revised FIG. 3(b), and respectfully asserts that the rejection has been accommodated. Specifically, Applicant has corrected FIG. 3(b) to properly depict that the carry in signal CI 104 is exclusively "OR"ed with the P signal 101 using the logical exclusive "OR" circuit 112 (*see* specification page 7, lines 21 – 22).

In the Specification

The Office Action indicates that the disclosure stands objected to because "PKG" purportedly is not clearly defined. Specifically, the Office Action indicates that a clear definition of the term "PKG" is required. As set forth above, Applicant has amended the specification to specifically recite that PKG is an acronym for Propagate-Kill-Generate. Applicant respectfully asserts that the addition of this language does not constitute new matter as the terms "propagate", "kill" and "generate" are recited with respect to the constituent letters of the acronym "PKG" in the Brief Description of the Drawings section of the originally filed application. Specifically, Applicant respectfully refers the Examiner to the brief description of FIGs. 2(b) – 2(d).

Additionally, Applicant has expressly recited that "a PKG input is provided by a PKG recoding operation that involves recoding logic values" and then redirects the reader to FIG. 1, which is a table illustrating a PKG encoding method. In redirecting the reader's attention to FIG. 1, Applicant has copied language from the written description appearing at page 1, lines 19 – 22 and respectfully asserts that this amendment to the specification adds no new matter.

Based on the foregoing, Applicant respectfully asserts that the requirement for a "clear definition of the term "PKG'" has been accommodated.

Rejections Under 35 U.S.C. 112

The Office Action indicates that claims 1 – 21 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Office Action indicates that the term "PKG value" is mentioned throughout the claims without particularly pointing out the exact PKG value or values. As set forth above, Applicant has amended the claims and respectfully asserts that the rejections have been accommodated.

Rejections Under 35 U.S.C. 102

The Office Action indicates that claims 1, 3 – 5, 7 – 9, 11, 13 – 15, 17 and 19 – 21 stand rejected under 35 U.S.C. 102(e) as being anticipated by *Inoue*. Applicant respectfully asserts that *Inoue* is legally deficient for the purpose of anticipating any of the aforementioned claims as *Inoue* does not teach, disclose or even suggest the use of PKG recoded numbers. In this regard, Applicant respectfully asserts that the amendments contained herein, which clearly define the term "PKG" has rendered the use of *Inoue* as a reference for rejecting the pending claims under 35 U.S.C. 102 improper. Because each of the aforementioned claims recites the use of at least one PKG value of a PKG recoded number, Applicant respectfully asserts that *Inoue* is legally deficient for anticipating any of the pending claims and respectfully requests that the rejection be withdrawn.

Rejections Under 35 U.S.C. 103

The Office Action indicates that claims 2, 6, 10, 12, 16 and 18 stand rejected under 35 U.S.C. 103(a) as being obvious over *Inoue* in view of *Miller*. As mentioned before, Applicant respectfully asserts that *Inoue* does not teach, disclose or otherwise suggest the use of even one PKG value of a PKG recoded number. Additionally, *Miller* is inadequate for remedying the deficiencies of *Inoue*. Specifically, *Miller* also does not teach, disclose or otherwise suggest the use of even one PKG value of a PKG recoded number. Therefore, Applicant respectfully asserts that the rejection under *Inoue* in view of *Miller* is no longer proper and that the claims are in condition for allowance.

Prior Art Made of Record

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1 – 21 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington D.C. 20231, on 10/31/02.

Stephanie Bailey
Signature

ANNOTATED VERSION OF MODIFIED SPECIFICATION TO SHOW CHANGES MADE

The following is a marked-up version of the amended specification, with the language that is underlined ("___") being added and the language that is enclosed within brackets ("[ ]") being deleted:

Page 7, line 1:

Illustrated in Fig. 3A is a block diagram of a possible example of a carry save adder 100 redesigned for performing addition on a newly encoded propagate, kill, generate (PKG) input and a traditional binary bit. A PKG input is provided by a PKG recoding operation that involves recoding logic values. As mentioned before, illustrated in FIG. 1 is a recoding table 2 illustrating the encoding of two logical values into mousetrap logic. The mousetrap logic values are then encoded into PKG recoding values to reduce the number of wires routed over an integrated circuit from four wires to three wires. As can be seen in FIG. 3A, the P 101, K 102 and G 103 signals are received by the modified carry save adder 100. The P 101, K 102 and G 103 signals are input along with carry-in signal CI 104, representing one traditional binary bit carry-in number.

ANNOTATED VERSION OF MODIFIED CLAIMS TO SHOW CHANGES MADE

The following is a marked-up version of the claims with the language that is underlined ("___") being added and the language that is enclosed within brackets ("[ ]") being deleted:

1. (Once Amended) An apparatus performing the addition of a PKG recoded number, said apparatus comprising:

a circuitry configured to receive at least a first value and a second value, wherein said second value is at least one of a P value, a K value, and a G value of a PKG [value] recoded number; and

wherein said circuitry generates a sum value and a carry value.

3. (Once Amended) The apparatus of claim 1, wherein said circuitry further comprises:

a first adder configured to add said first value and said second [PKG] value, said first adder generates a carry-out value and at least one of a P value, a K value and G value of a PKG [value] recoded number [and a carry-out value].

5. (Once Amended) The apparatus of claim 3, wherein said first value is at least one of a P value, a K value and a G value of a PKG [value] recoded number.

6. (Once Amended) The apparatus of claim 1, further comprising:

a recoder configured to convert at least one dual rail encoded value into said second [PKG] value.

7. (Once Amended) A method for performing the addition of PKG recoded numbers, comprising the steps of:

receiving a first value;

receiving a second [PKG] value, wherein said second value is at least one of a P value, a K value and a G value of a PKG recoded number; and

generating a sum value and a carry value from said first value and said second [PKG] value.

8. (Once Amended) The method of claim 7, further comprising the steps of:

adding said first value and said second [PKG] value;

generating a first result including at least one of a P value, a K value and a G value [PKG] value from said adding; and

generating a first carry-out value from said adding.

9. (Once Amended) The method of claim 8, further comprising the steps of:

adding said first result [PKG value] and a carry-in value;

generating a final sum value from said adding; and

generating a final carry-out value from said adding.

11. (Once Amended) The method of claim 8, wherein said first value is at least one of a P value, a K value and a G value of a PKG [value] recoded number.

12. (Once Amended) The method of claim 7, further comprising the step of:

converting at least one dual rail encoded value into said second [PKG] value.

13. (Once Amended) An apparatus for apparatus performing the addition of PKG recoded number, said apparatus comprising:

means for receiving a first value;

means for receiving a second [PKG] value, said second value including at least one of a P value, a K value and G value of a PKG recoded number ; and

means for generating a sum value and a carry value from said first [PKG] value and said second [PKG] value.

14. (Once Amended) The apparatus of claim 13, further comprising:

means for adding said first value and said second [PKG] value to generate a first result [PKG value] and a first carry-out value.

15. (Once Amended) The apparatus of claim 14, further comprising:

means for adding said first result [PKG value] and a carry-in value to generate a final sum value and a final carry-out value.

17. (Once Amended) The apparatus of claim 15, wherein said first value is at least one of a P value, a K value and a G value of a PKG [value] recoded number.

18. (Once Amended) The apparatus of claim 13, further comprising:

means for converting at least one dual rail encoded value into said second [PKG] value.

19. (Once Amended) An apparatus performing the addition of PKG recoded numbers, said apparatus comprising:

a circuitry configured to receive at least one of a P value, a K value and a G value of a first PKG recoded number and at least one of a P value, a K value and a G value of a second PKG recoded number [two PKG values]; and

wherein said circuitry generates a carry value and [PKG] at least one of a P value, a K value and a G value [and a carry value].

20. (Once Amended) A method for performing the addition of PKG recoded numbers, comprising the steps of:

receiving at least one of a P value, a K value and a G value of a first PKG [value] recoded number;

receiving at least one of a P value, a K value and a G value of a second PKG [value] recoded number; and

generating a PKG sum value and a carry value [from said first PKG value the and said second PKG] the values received.

21. (Once Amended) An apparatus for apparatus performing the addition of PKG recoded number, said apparatus comprising:

means for receiving at least one of a P value, a K value and a G value of a first PKG [value]recoded number;

means for receiving at least one of a P value, a K value and a G value of a second PKG [value] recoded number; and

means for generating at least one of a P value, a K value and a G value of a PKG sum [value] recoded number and a carry value from [addition of said first PKG value and second PKG value]the values received.

FIG. 3A

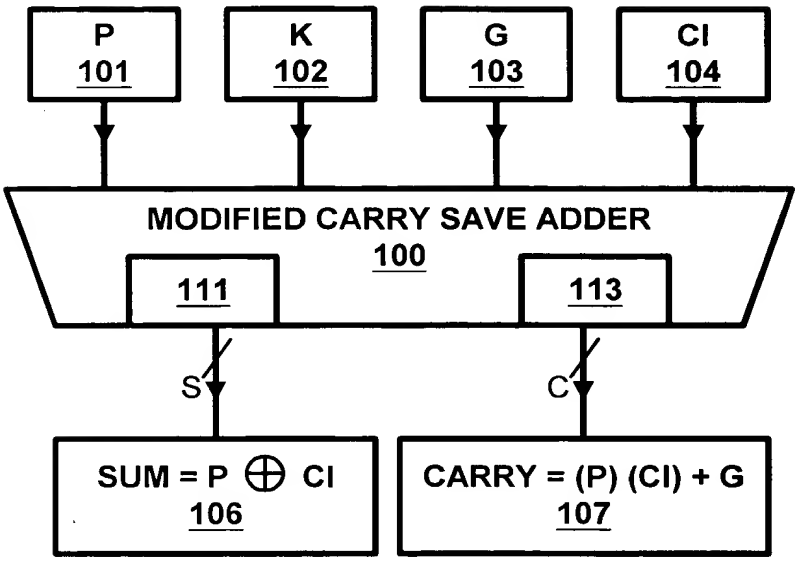

FIG. 3B

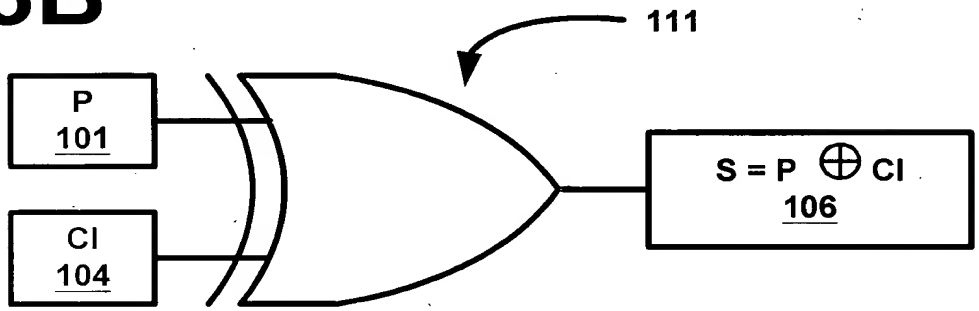

FIG. 3C